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Patent and Trademark Office U.S. DEPARTMENT OF COMMERCE

1449/PTO

U.S. Department of Commerce
Patent and Trademark Office

Application No. : 10/046,792

Filing Date : January 15, 2002

First Named Inventor: H. NATSUME

Group Art Unit : 2811

Examiner Name :

Attorney Docket No. : NECW 19.349

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Sheet 1 of 1

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No. ¹	U.S. Patent Document	Kind Code if known ²	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns Lines Where Relevant Passages or Relevant Figures Appear
JN		6,091,628		KIM	07/18/2000	

FOREIGN DOCUMENTS

Examiner Initials	Cite No. ¹	Foreign Patent Document Office ³ Number ⁴ Kind Code ⁵ (if known)	Country	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns Lines Where Relevant Passages or Relevant Figures Appear
JN		0 104 616	EP	SIEMENS AG (DE)	04/04/1984	

Other Prior Art-Non-Patent Literature Documents

Examiner Initials JN	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), data, page(s), volume-issue number(s), publisher, country, where published, source.	Applicant check her if English language translation attached
Examiner Signature JOSEPH NGUYEN	Date Considered 4/7/03		

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JN		11-251457	JP	Motorola Inc	09/17/1999	
		07-099255	JP	Hitachi Ltd.	04/11/1995	
		09-260510	JP	Hitachi Ltd.	10/03/1997	

Other Prior Art-Non Patent Literature Documents

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), data, page(s), volume-issue number(s), publisher, country, where published, source.	Applicant check her if English language translation attached
JN		INOHARA et al. Highly Scalable and Fully Logic Compatible SRAM Cell Technology with Metal Damascene Process and W Local Interconnect. Symposium on VLSI Technology Digest of Technical Papers pp.64-65, 1998	
		OOTSUKA et al. A Novel .20 μm Full CMOS SRAM Cell Using Stacked Cross Couple with Enhanced Soft Error Immunity. IEDM 1998	

Examiner Signature	JOSEPH MUYEN	Date Considered	4/7/03
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